

Sheet 1 of 1

FORM PTO-1449
(REV. 7-80)U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICEATTY. DOCKET NO.
NIT-201-03SERIAL NO.
10/827,291LIST OF DOCUMENTS CITED BY APPLICANT
(Use several sheets if necessary)APPLICANT
N. KATOH et alFILING DATE
April 20, 2004

GROUP

U.S. PATENT DOCUMENTS

* EXAMINER INITIAL		DOCUMENT	DATE	NAME	CLASS	SUBCLASS	FILING DATE (If Appropriate)
AT	AA	5,486,774	01/23/96	Douseki et al (which claims priority from JP 05-218850, copy enclosed			
	AB						
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FOREIGN PATENT DOCUMENTS

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OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

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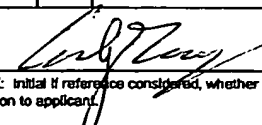
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LIST OF DOCUMENTS CITED BY APPLICANT (Use several sheets if necessary)				APPLICANT N. KATOH et al		GROUP		
				FILING DATE April 20, 2004				
U.S. PATENT DOCUMENTS								
* EXAMINER INITIAL		DOCUMENT	DATE	NAME	CLASS	SUBCLASS	FILING DATE (If Appropriate)	
AT	AA	5,774,367	06/30/98	Reyes et al (which claims priority from JP 09-045785, copy enclosed)				
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LIST OF DOCUMENTS CITED BY APPLICANT <i>(Use several sheets if necessary)</i>				APPLICANT			
				N. KATOH et al			
				FILING DATE		GROUP	
		April 20, 2004					
U.S. PATENT DOCUMENTS							
* EXAMINER INITIAL	DOCUMENT	DATE	NAME	CLASS	SUBCLASS	FILING DATE (If Appropriate)	
<i>AT</i> ↓	AA	5,774,367	06/30/98	Reyes et al			
	AB	5,614,847	03/1997	Kawahara et al			
	AC	6,118,309	09/2000	Akamatsu et al			
	AD	6,222,410	04/2001	Seno			
	AE	5,898,742	04/1999	Van Der Werf, Albert			
	AF	6,209,122	03/2001	Jyu et al			
	AG	5,880,967	03/1999	Jyu et al			
	AH	6,272,668	08/2001	Teene, Andres R.			
	AI	6,035,106	03/2000	Carruthers et al			
	AJ	5,872,716	02/1999	Yano et al			
	AK	6,009,248	12/1999	Sato et al			
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	AP					<input type="checkbox"/>	<input type="checkbox"/>
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)							
<i>AT</i> ↓	AR	S. Mutoh et al, "1-V Power Supply High-Speed Digital Circuit Technology with Multithreshold-Voltage CMOS", IEEE JOURNAL OF SOLID-STATE CIRCUITS, Vol. 30, No. 8, August 1995, pp. 847-854.					
	AS	T. Sakata et al, "Subthreshold-Current Reduction Circuits for Multi-Gigabit DRAM's", 1993 SYMPOSIUM ON VLSI CIRCUITS DIGEST OF TECHNICAL PAPERS, May 1993, pp. 45-46.					
	AT	Uebel et al, "A Timing Model for VLSI CMOS Circuits Verification and Optimization", 1994 IEEE International Symposium on Circuits and Systems, Vol. 1, May 30, 1994, pp. 439-442.					
EXAMINER				DATE CONSIDERED			
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FORM PTO-1449 (REV. 7-80)		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. NIT-201-03	SERIAL NO. <u>1082729.1</u>		
LIST OF DOCUMENTS CITED BY APPLICANT <i>(Use several sheets if necessary)</i>				APPLICANT N. KATOH et al			
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* EXAMINER INITIAL	DOCUMENT	DATE	NAME	CLASS	SUBCLASS	FILING DATE (If Appropriate)	
<u>AT</u> <div style="border-left: 1px solid black; height: 100px; margin: 0 auto; width: 20px;"></div>	AA	5,774,367	06/1998	Reyes et al			
	AB	6,167,554	12/2000	Ishikawa et al			
	AC	5,983,007	11/1999	Agrawal, Vishwani Deo			
	AD	6,038,381	03/2000	Munch et al			
	AE	5,654,898	08/1997	Roetcisoender et al			
	AF	6,209,123	03/2001	Maziasz et al			
	AG	6,006,024	12/1999	Guruswamy et al			
	AH	5,984,510	11/1999	Guruswamy et al			
	AI	5,822,214	10/1998	Rostoker et al			
	AJ	4,839,820	06/1989	Kinoshita et al			
	↓	AK	4,656,592	04/1987	Spaenenburg et al		
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<u>AT</u> <div style="border-left: 1px solid black; height: 100px; margin: 0 auto; width: 20px;"></div>	AR	Daga et al, "Delay Modelling Improvement for Low Voltage Applications", Proceedings of European Design Automation Conference, Sept. 18, 1995, pp. 216-221.					
	AS	Rofail et al, "Delay Time Sensitivity Analysis of Multi-Generation BiCMOS Digital Circuits", IEEE Proceedings of Circuits, Devices and Systems, Vol. 144, No. 2, Apr. 1997, pp. 60-67.					
<div style="border-left: 1px solid black; height: 100px; margin: 0 auto; width: 20px;"></div>	AT	NA84035023, "Logic Signal Delay Circuit", IBM Technical Disclosure Bulletin, Vol. 26, No. 10A, Mar. 1984, pp. 5023-5025.					
EXAMINER <u>[Signature]</u>				DATE CONSIDERED <u>6/15/06</u>			

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* EXAMINER INITIAL	DOCUMENT	DATE	NAME	CLASS	SUBCLASS	FILING DATE (If Appropriate)
AT	AA	5,831,864	11/1998	Raghunathan et al		
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AT	AR	NB9001420, "Buffer Circuit with Delayed Rising or Falling Transition for Pulsewidth Skew Control", IBM Technical Disclosure Bulletin, Vol. 32, No. 8B, Jan. 1990, pp. 420-421.				
AT	AS	NN87044929, "High Noise Immunity CMOS Driver", IBM Technical Disclosure Bulletin, Vol. 29, No. 11, Apr. 1987, pp. 4929-4930.				
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